

WHAT IS CLAIMED IS:

- Sub A1*
1. A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal VIN is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring, wherein a node arranged in the vicinity of an input terminal of the gate circuit connected to an input terminal of the driver circuit and an end of the first long-distance wiring is connected by a second long-distance wiring and a speed-increasing circuit.
2. The semiconductor integrated circuit device as claimed in Claim 1, wherein the speed-increasing circuit includes a PMOS transistor.
3. The semiconductor integrated circuit device as claimed in Claim 1, wherein the speed-increasing circuit includes an NMOS transistor and a buffer circuit is inserted at an input side of the second-long distance wiring.
4. The semiconductor integrated circuit device as claimed in Claim 1, wherein the speed-increasing circuit includes a CMOS inverter having a PMOS transistor and an NMOS transistor.
5. The semiconductor integrated circuit device as claimed in Claim 1, wherein a plurality of speed-increasing circuits are additionally inserted between

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an intermediate position of the second long-distance wiring and the vicinity of the input terminal of the gate circuit connected to a position corresponding to that intermediate position.

SUB A2

6. The semiconductor integrated circuit device as claimed in Claim 1, wherein a plurality of buffer circuits and are inserted at the input side of the second long-distance wiring.

7. The semiconductor integrated circuit device as claimed in Claim 1, wherein a buffer circuit is inserted at the input side of the second long-distance wiring, and a buffer circuit is inserted at the output side of the second long-distance wiring.

SUB C2

8. The semiconductor integrated circuit device as claimed in Claim 1, wherein the input signal VIN is realized by a word line selecting signal; the driver circuit is realized by a word line driver; the first long-distance wiring is realized by a word line WL; and the gate circuits are realized by memory cells.

9. The semiconductor integrated circuit device as claimed in Claim 1, wherein the input signal VIN is realized by a clock input signal VCK; the driver circuit is realized by a clock driver; and the gate circuits are realized by flip-flop circuits.

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